

A Calibration Scheme for Stability of Self-biased Ring Amplifier

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Abstract. This paper presents a calibration scheme to enhance the robustness of the Self-Biased Ring Amplifier (SBRA) under PVT variations. As the ring amplifier is developed based on a ring oscillator structure, it can easily oscillate under PVT variations. The proposed calibration method utilizes an Oscillation Detection Circuit (ODC) with a close loop control of a Programmable Resistor Array Circuit (PRAC) to adjust the dead-zone (stability region), thus stabilizing the SBRA. The introduced ODC and PRAC have little influence on the power efficiency as well as hardware overhead. Based on a 1.5 bit/stage Multiplying Digital to Analog Converter (MDAC) circuit setup, the simulation shows that the proposed method can stabilize the ring amplifier in the range of 0°C to 85°C at all corners.

1. Introduction

In advance nanometer CMOS technology, it constitutes a challenge to design a power efficient operational trans-conductance amplifier (OTA) for high accuracy switched-capacitor circuits in low supply voltage with traditional topologies, such as folded-cascode and multi-stage. The comparator-based circuits and inverter-based amplifiers tend to be more power efficient and compactable to technology scaling because of their Class-A/B (even Class C) type of operation, scalability and large output swing [1]-[2]. However, a single stage inverter (with peak gain smaller than 45dB) from [2] does not meet the high accuracy requirement of a pipeline ADC with 10bit or higher resolution. In [3], a two-stage inverter-based amplifier has been proposed but the need of compensation and a class-A output stage without rail to rail swing limit its power efficiency. The ring amplifier proposed in [4], which is composed of 3 stage inverters as depicted in Fig. 1 (a), combines the advantages of the comparator-based and inverter-based circuits with slew-based charging, rail-to-rail output swing and without needing compensation, thus guaranteeing its good power efficiency.

Nevertheless, like the inverter-based amplifier, the ring amplifier is typically prone to PVT variations (due to low power supply rejection ratio, temperature/input dependent bias current etc.). For inverter-based amplifier, methods [3], [5]-[6] have been proposed to address this problem which focuses on the biasing techniques but sacrifices the power efficiency in certain level. For the ring amplifier, [7] proposes a self-biased ring amplifier (SBRA), as depicted in Fig. 1 (b), which introduces biasing voltage rather than using a capacitor. A resistor R_S is inserted between the drain of M_{p2} and M_{n2} in the 2nd stage which generates voltages V_{BP2} and V_{BN2} to control the range of the dead-zone. The advantage of this implementation over the original is related with the fact that V_{BP2} and V_{BN2} can track the variation of the supply voltage in certain level [7] allowing the adjustment of the range of the dead-zone. However, the process and temperature variations are still not addressed which can also induce stability problems in the ring amplifier.

In this paper, a calibration method is proposed which aims to stabilize the SBRA under the PVT variations without degrading much its power efficiency. The calibration scheme adopts analog oscillation detection circuit with digital feedback control that dynamically controls the dead-zone through the tunable resistor in the 2nd stage to stabilize the SBRA. The paper is organized as follows, in section 2, design considerations and characteristics of the SBRA are discussed. The proposed idea is detailed in section 3. In section 4, simulation results are reported, with the conclusions drawn in section 5.

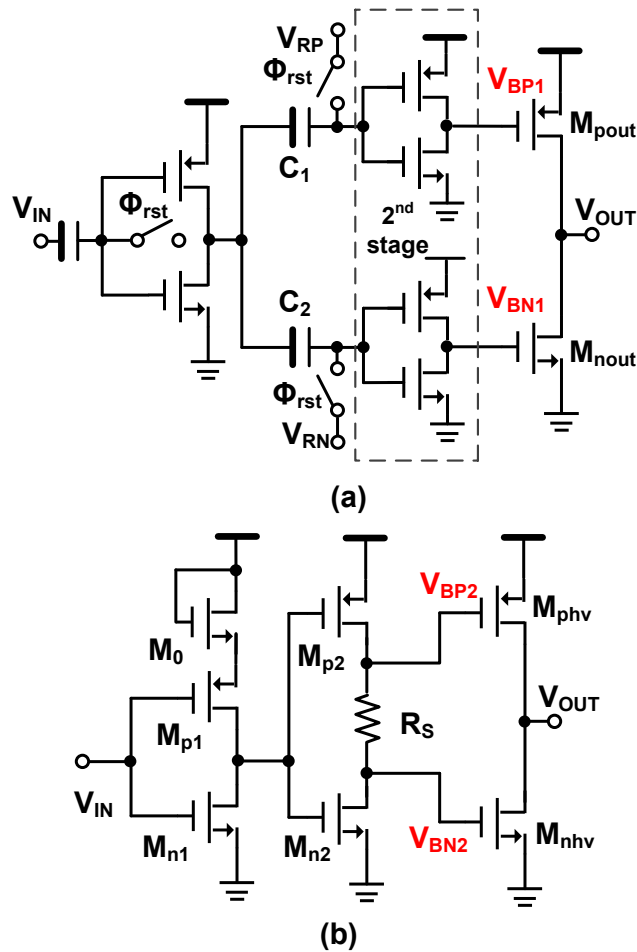


Figure 1 Ring amplifier (a) proposed in [4] (b) self-biased ring amplifier (SBRA) [7].

2. Design Consideration of Self-Biased Ring Amplifier (SBRA)

In this section, the design considerations of the SBRA are reviewed and its characteristics under PVT variation are described.

2.1. Selection of R_S

As discussed in [4], when the ring amplifier performs amplification, it starts from the initial ramping phase, then oscillates but gradually stabilizes until entering the stabilization phase. In the initial ramping phase, the output transistor $M_{\text{pout}}/M_{\text{nout}}$ (in Fig. 1 (a)) operates as a maximum-biased (by VDD or GND) current source because $V_{\text{BN1}}/V_{\text{BP1}}$ has a rail-to-rail voltage swing. Hence, the speed limitation mainly lies in the stabilization phase with limited power consumption. By enlarging the dead-zone range, the time required to stabilize the amplifier is reduced, so the speed of the ring amplifier will be increased. For SBRA, when the dead-zone is enlarged by having a higher value of R_S , it simultaneously reduces the time to be stabilized and increases the duration in the initial ramping phase. This is due to the larger voltage drop across R_S which reduces the voltage swing of $V_{\text{BN2}}/V_{\text{BP2}}$ leading to the maximum bias voltage for $M_{\text{phv}}/M_{\text{nhv}}$ in this phase. As the bias voltage drops, the charging current shrinks and the charging time is increased. If R_S is too large, the time spent in the initial ramp phase will be dominant and the SBRA will be slow. visible to keep all the given values.

In Fig. 2, a 1.5 bit/stage MDAC using two self-biased ring amplifiers to form a pseudo-differential circuit is illustrated which will be carried along as the base of the testing setup here. For simplicity, only half of the circuit is shown with the information about the phases. This circuit operates in two main clock phases: ϕ_1 and ϕ_2 . During ϕ_1 with the auto-zeroing operation, the input and output of SBRA are connected and storing the offset in C_C . Since the load (C_L) is absent in this phase, C_{aid} is introduced to ensure the stability [7]. A reset phase ϕ_{rst} is inserted before ϕ_1 to make the starting point of auto-zeroing independent of the previous input. The signals' behavior at the SBRA's output in ϕ_2 is illustrated in Fig. 3 with three different values of R_S . It can be observed that the output oscillates with the smallest value of R_S (curve A). On the other hand, the settling of the MDAC becomes very slow for the largest R_S (curve C). For the amplifier to be stable, R_S needs to be increased but limited by the finite settling time requirement. Then, the choice of the R_S value implies a trade-off between speed and stability in the ring amplifier.

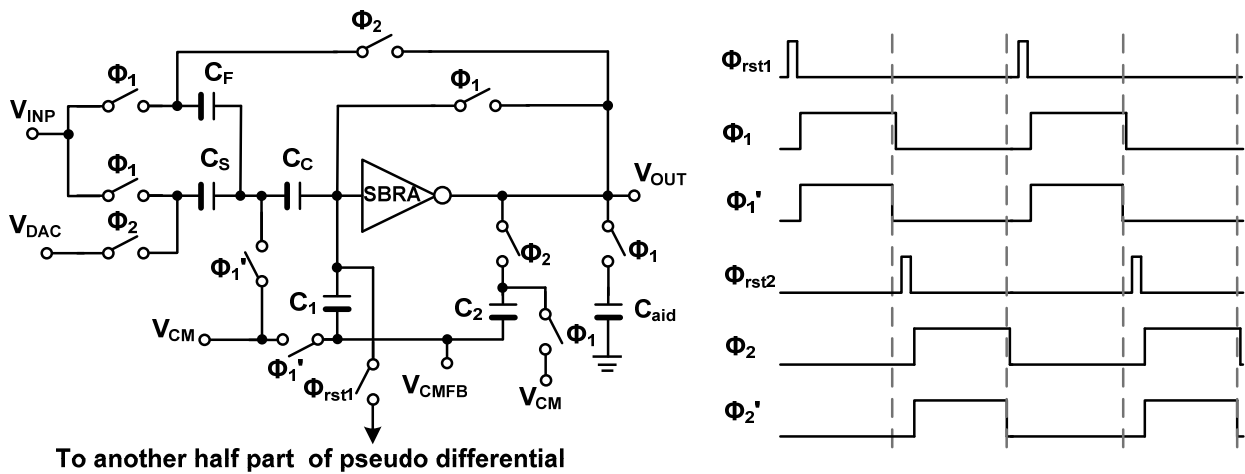


Figure 2 1.5 bit MDAC using SBRA implanted in a pseudo-differential structure.

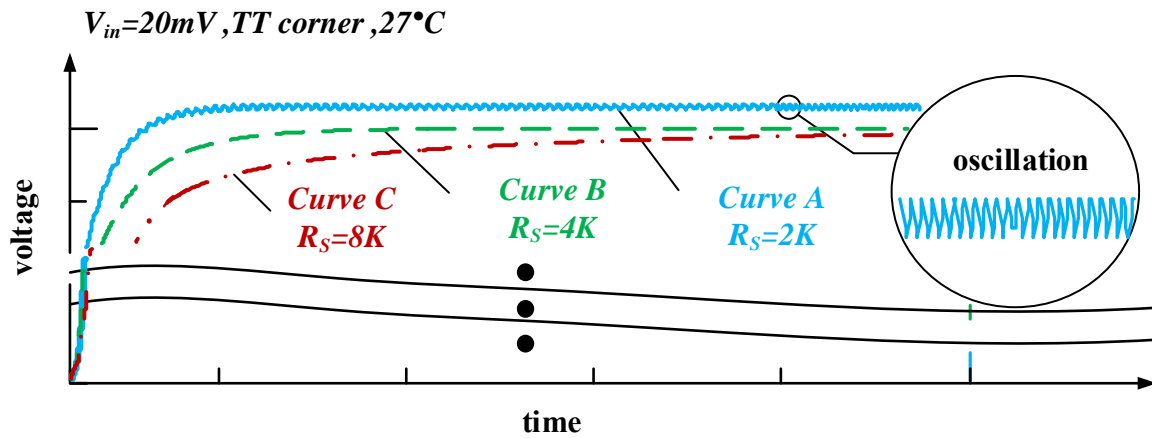


Figure 3 Settling behavior of SBRA with different R_S .

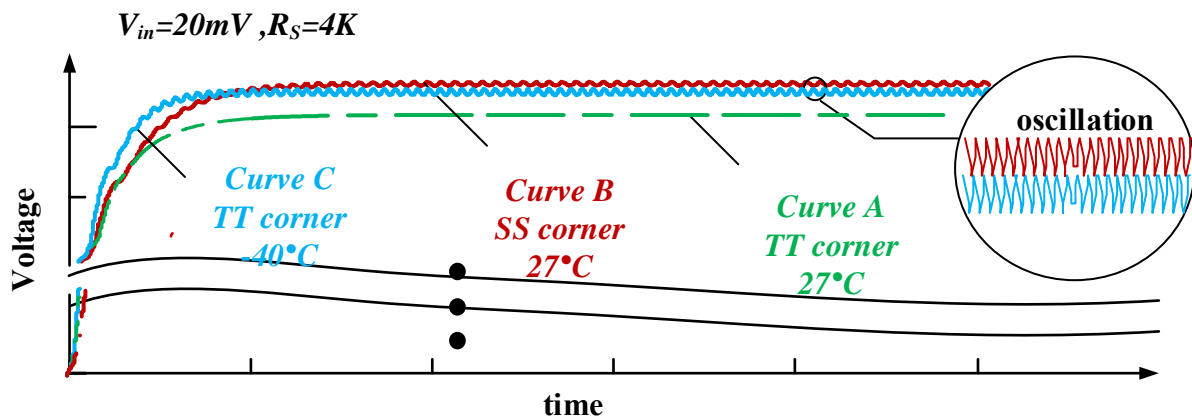


Figure 4 Settling behavior of SBRA with same R_S under PT.

2.2. Characteristics of SBRA under PVT Variations

As mentioned in section I, SBRA is still prone to process and temperature variations. A certain range of R_S values allows the amplifier to be stable in a typical (TT) corner at room temperature (27°C) and its transient response can be plotted as curve A in Fig. 4. After changing to SS corner and keeping 27°C with the same value of R_S , the amplifier oscillates as illustrated in curve B. By varying the temperature to -40°C at TT corner, with the same value of R_S , it also leads to oscillation as shown in curve C.

For the traditional inverter based amplifier, although the PVT variations lead to change in GBW, gain, etc., the amplifier is still stable. However, for the ring amplifier, the PVT variations can lead to oscillation which is a serious drawback for the MDAC. This is the unique feature of the ring amplifier which needs to be handled to enhance the robustness of the circuit under PVT variations.

3. Proposed Calibration Method

To insure the stability of SBRA under the temperature and process variations, a calibration method is proposed with an operation principle illustrated in Fig. 5. Firstly, the MDAC using SBRA is configured in the calibration Mode: perform the normal operation of the MDAC, reset the smallest value of the programmable resistor R_P which is in a Programmable Resistor Array Circuit (PRAC) parallel connected with R_S and connect the Oscillation Detection Circuit (ODC) to V_{CMFB} (Fig. 2). Secondly, when the MDAC performs the sample and amplification, the ODC will sample the value of V_{CMFB} in every amplification phase and generates a digital output. After N cycles (using a digital counter), N outputs ($D_1 \dots D_N$) are generated. Thirdly, these N digital outputs are compared: if they are all the same, it means the SBRA is stable and then the calibration will stop and PRAC will increase R_P by one more step to leave margins for the suddenly environment changed such as supply variation. If not, the SBRA will be oscillating and a rising edge of the signal O_{SC} will be generated and passed to PRAC. When the PRAC receives one rising edge of O_{SC} , the value of R_P will increase by one step, thus enlarging the total resistance of R_P/R_S as well as the dead-zone. In this work, the same N steps are designed for the programmable resistor. After that, D_1 to D_N will be clear and ODC starts a new round of detection until D_1 to D_N are the same.

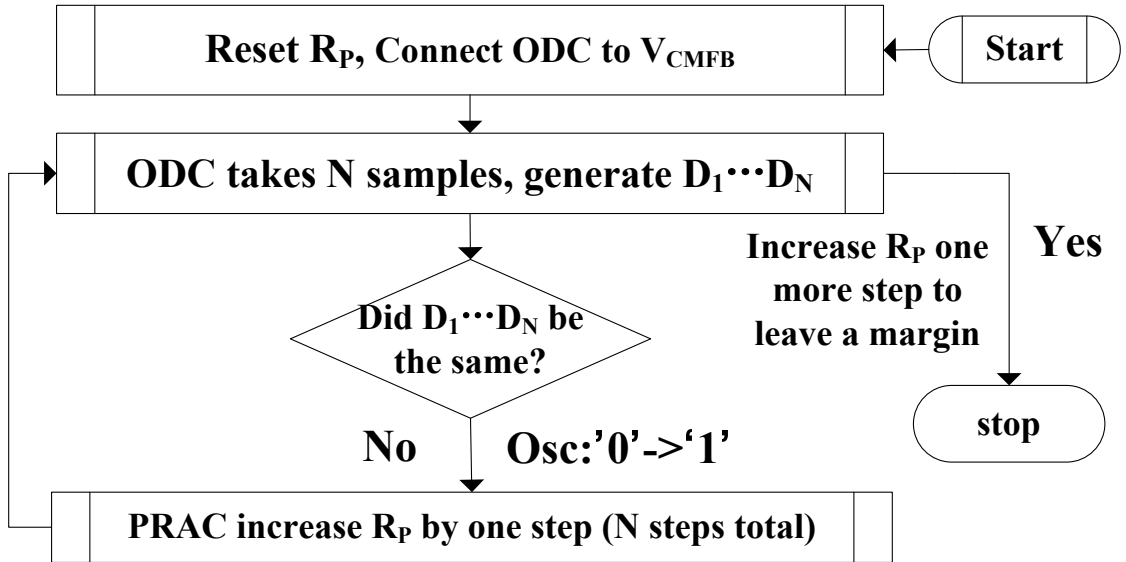


Figure 5 Procedure of the proposed calibration method.

3.1. Oscillation Detection Circuit (ODC)

To detect the oscillation, V_{CMFB} is chosen due to the oscillation and its value is always around a constant voltage level: V_{CM} . Hence, V_{CMFB} with V_{CM} can be compared and a clock signal is generated that can be detected in the digital domain. For other nodes like the output nodes; however, oscillation will occur around different voltage levels according to its input, then imposing a harder comparison. Ideally, comparing V_{CMFB} with V_{CM} needs a high-speed comparator with an operating frequency that should be at least twice the value of the oscillation. This will consume huge power and reduces energy efficiency. Therefore, a time shift sampling scheme (TSSS) is proposed to address this issue.

As illustrated in Fig. 6 (a), when performing the calibration, the TSSS will capture one sample of V_{CMFB} in one amplification phase and does the comparison. After $T_{TSSS} + \Delta t_d$ which is equal to one clock period of ϕ_2 plus a tiny time difference Δt_d where Δt_d is twice smaller than the

oscillation period, TSSS will take another sample. Then, after every sample, the comparator will have $T_{TSSS} + \Delta t_d$ to perform the comparison. TSSS greatly reduces the speed requirement of the comparator and allows more time for higher accuracy comparison (such as adding capacitors at the comparator's outputs to reduce the overall comparator's noise). Eventually, a simple Strong-Arm architecture [8] is used due to its simplicity and background offset calibration [9] is needed for PVT consideration. The design of comparator needs the cooperation of the appropriate step size of the programmable resistor to maintain a good calibration accuracy which will be discussed in the next part. The block diagram of ODC is depicted in Fig. 6 (a).

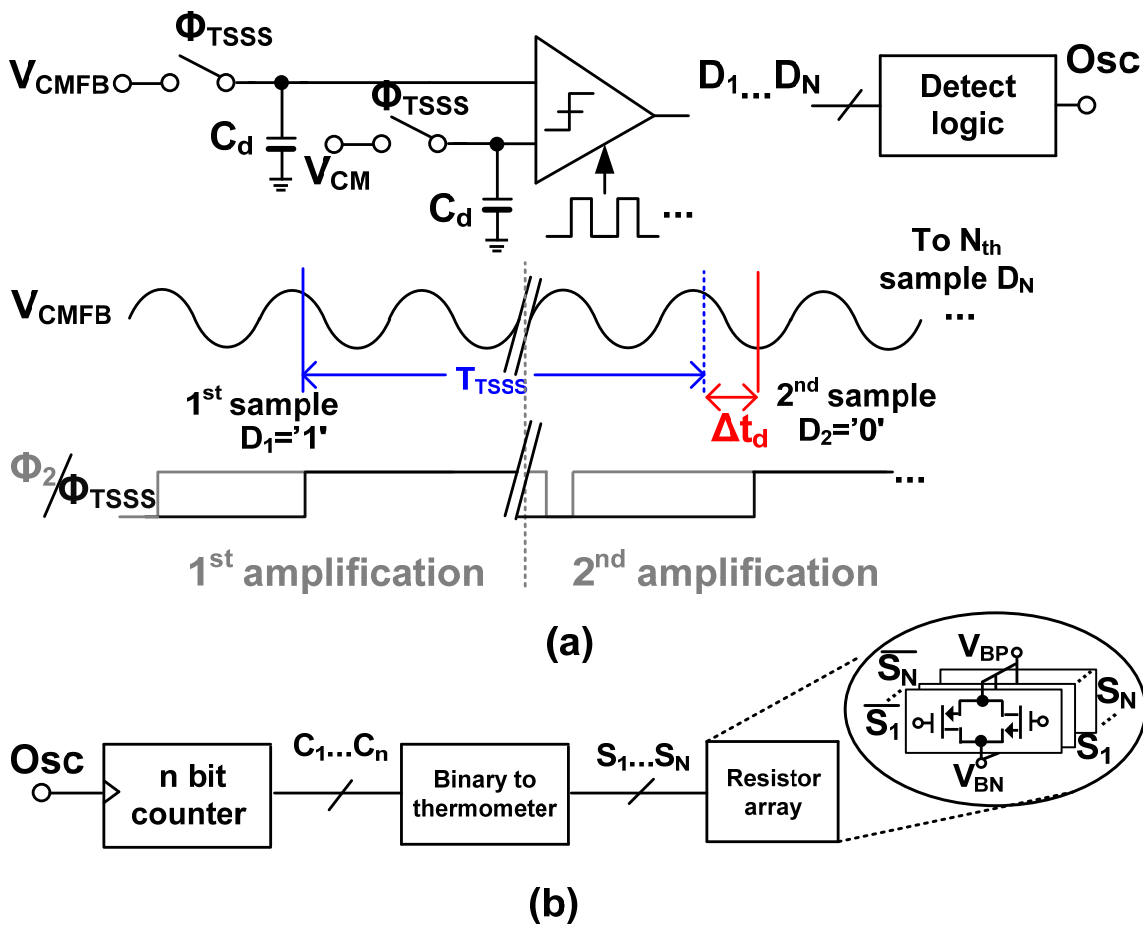


Figure 6 The block diagram of ODC (a) and PRAC (b).

3.2. Programmable Resistor Array Circuit (PRAC)

After the ODC indicates the oscillation, the R_p should be increased to stabilize the amplifier. However, aggressively increasing R_p will slow down the settling of the amplifier. Then, the best way to follow to ensure stabilization is to increase the value of R_p in small steps until a relative optimum point is reached (stable but not too slow). The lower bound of the step size is limited by the detectable oscillation swing determined by the oscillation detection circuit, mainly the residual offset voltage of the comparator after calibration. In this design, the programmable resistor R_p is

realized by group of CMOS switches. The steps are controlled by n binary control bits ($C_1 \dots C_n$) which are equal to N in this design. The block diagram of PRAC is depicted in Fig. 6 (b).

4. Simulation Results

The 1.5 bit/stage MDAC platform with 10-bit accuracy is setup to perform the simulation in 65 nm technology. C_F and C_S are 200fF. C_C is 400fF. The supply voltage is 1.2V. The transistor sizes of the SBRA in Fig. 1 (b) are summarized in Table I.

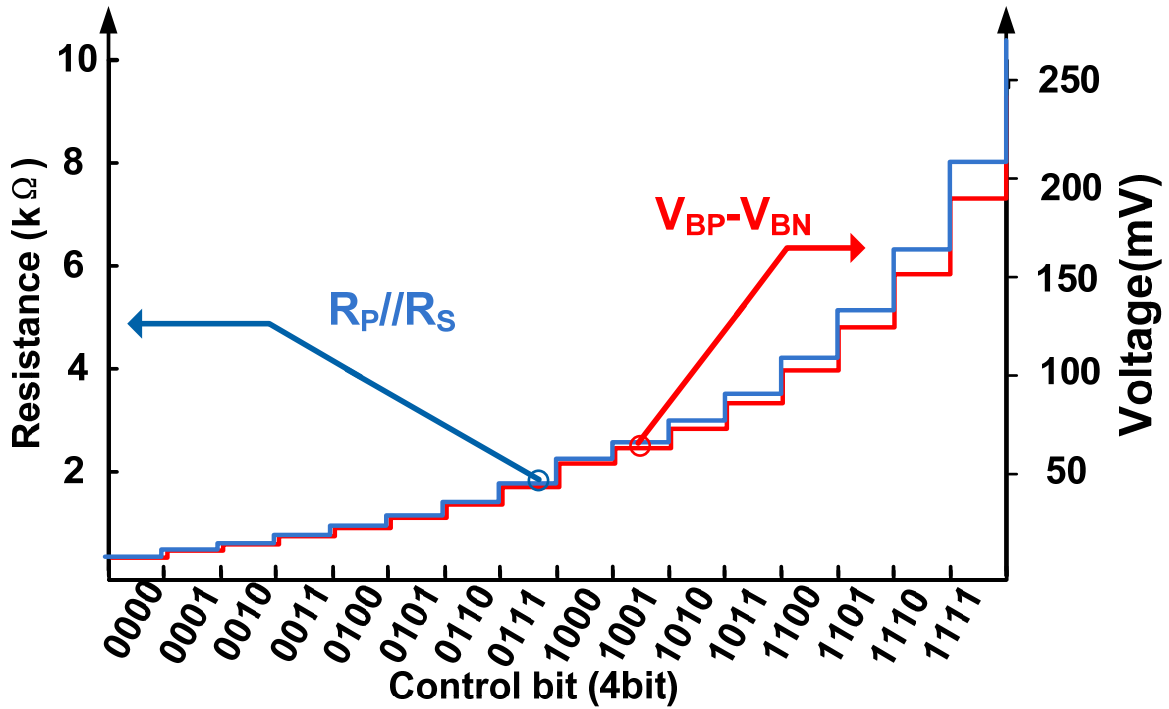


Figure 7 Step size of programmable resistor and $V_{BP}-V_{BN}$.

N is chosen as 16 and the programmable resistor array is controlled by $n=4$ digital bits. Fig. 7 illustrates the step size of the resistance and the difference between V_{BP} and V_{BN} (dead-zone). It can be observed that the step size of the resistance is not a linear function of the control bit. This is since the step size requirement for a different range of R_S will be deviated. Especially in the SS corner with low temperature, the current in the 2nd stage is smaller than in the other corners. The largest R_S is needed to stabilize SBRA. Also, the step size should be proportionally increased to reduce the total step number. Thus, a gradually increased step size of the resistance is designed as the control bit increases. Fig. 8 shows the output waveform (differential) of the MDAC when a programmable resistor is controlled by different digital codes at $V_{in}=500mV$, SS corner, 0°C. By enlarging the value of the resistance for the dead-zone range, finally the SBRA is stable.

To demonstrate the effectiveness of the proposed calibration method, a design with only R_S (P+ poly resistor, around 9.8KΩ) to make SBRA being stable in all corners and temperature range is constructed for comparison. The simulation results for a fixed input voltage ($V_{in}=500mV$) are summarized in Table II. The simulations show that the proposed method has a speed variation from 50MS/s (FF, 85°C.) to 10MS/s (SS, 0°C). As reported in [6], for the simple inverter-based amplifier, the largest unity gain bandwidth is around 3 times over the smallest one under temperature

variations only. Such a large speed variation (compared with using traditional OTA being around $\pm 30\%$) is normal for the ring amplifier. And the proposed calibration method mainly addresses the PVT variations introduced stability problem which at least keeps the amplifier functional. The circuit with R_S only has a speed variation from 10MS/s (SS, 0°C) to 2 MS/s (FF, 85°C). In the worst-case scenario, the proposed method is 5x faster than the fixed R_S method. Eventually, the proposed calibration method can stabilize SBRA in the range of 0°C ~85°C at all corners. Wider temperature range can be archived by enlarging the tunable range of $R_p||R_S$ if necessary.

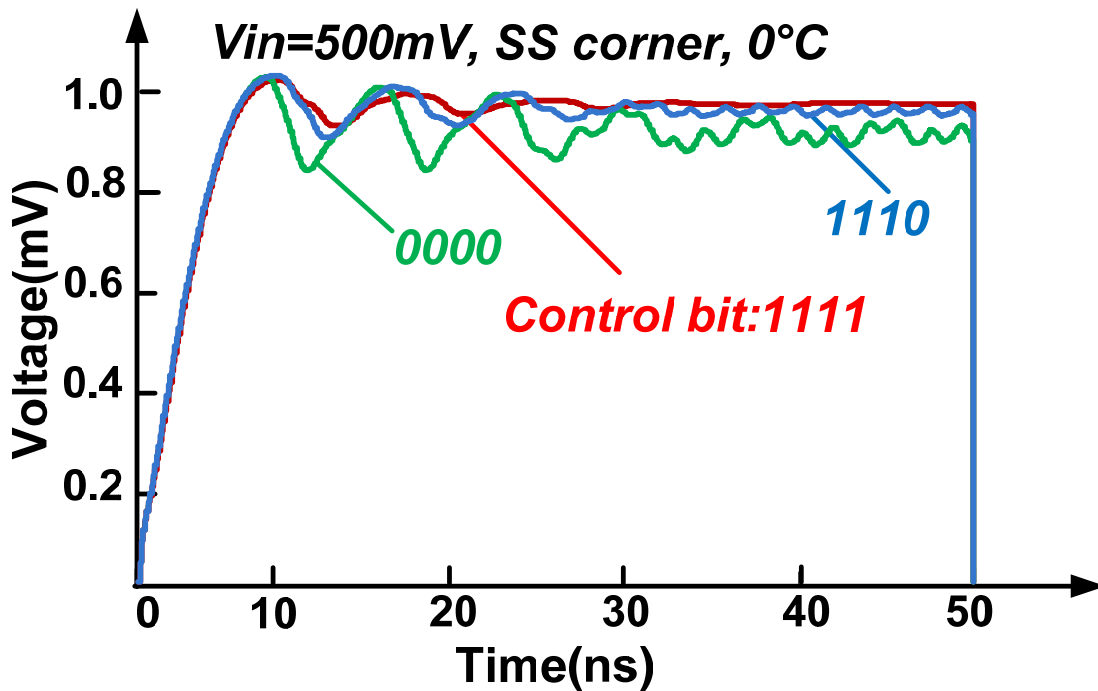


Figure 8 . MDAC output waveform under different control bit.

Table 1 Transistors Sizes.

Transistors/ Switches	Length(μm)/Width (μm)	Transistors/ Switches	Length(μm)/Width(μm)
M_0 (low V_{th})	24/0.1	M_{p1}	20/0.07
M_{n1}	10/0.07	M_{p2}	3.2/0.08
M_{n2}	1.6/0.08	M_{phv} (high V_{th})	1.2/0.18
M_{nhv} (high V_{th})	0.6/0.18		

Table 2 Simulation Results Summary.

	Process Corner and temperature		
	TT, 27°C	SS, -40°C	FF, 85°C
Proposed method	20 MS/s (63dB) Control bit:0000	10 MS/s (66dB) Control bit:1111	50 MS/s(61dB) Control bit:0000
Fixed R_S	6 MS/s (63dB)	10 MS/s (66dB)	2 MS/s (60dB)

5. Conclusions

A calibration method aiming to insure the stability of SBRA under PVT variations has been presented. Unlike the tuning circuit from [10] that operates in open loop, the proposed circuit operates automatically in close loop. Also, the calibration scheme eases the need of high speed dynamic comparator and only requires little additional digital circuitry which only has slight influence on the power efficiency of the ring amplifier. The proposed method is 5x faster than a fixed dead-zone design by constant R_S in the worst-case scenario.

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